



#40460
7-11-01

PATENT
ATT's Dkt: 2207/10607

#9A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

SOLOMON et al

Serial No.: 09/892,566

Filed: June 28, 2001

For: POWER REDUCTION FOR
PROCESSOR FRONT-END BY
CACHING DECODED
INSTRUCTIONS

Examiner: Not assigned

Art Unit: Not assigned

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Preliminary to examination of the above-identified application, please amend the application as follows:

IN THE CLAIMS:

Please amend the claims 19 and 20 as follows. A clean copy of the claims, as required by rule, are provided in the attached Appendix.

AI 19. (Amended) The cache of claim 4216, further comprising a field to store a next line pointer, indicating another way in the cache in which subsequent uops are likely to be found.

20. (Amended) The cache of claim 4216, wherein an offset field comprises a plurality of offset sub-fields, each sub-field corresponding to a UOP position in the cache line.